AMENDMENTS TO THE CLAIMS

1. (Currently amended) A receiving apparatus comprising:

at least one variable gain amplifier;

at least one level detection circuit, which detects at least one level output from said at least one variable gain amplifier;

at least one comparing circuit for comparing at least one reference level to said at least one output from said at least one level detection circuit;

at least one demodulator;

at least one binarizing circuit;

~~at least one gain switching detection circuit detecting switching of at least one gain of said at least one variable gain amplifier;~~

at least one slice level holding circuit holding at least one substantially constant value at least one slice level employed by said at least one binarizing circuit; and

at least one counter circuit;

wherein at least one gain of said at least one variable gain amplifier is switched based on at least one result of comparison by said at least one comparing circuit; and

wherein, when ~~switching of said at least one gain is detected by said at least one gain switching detection circuit,~~ said at least one gain is switched, said at least one counter circuit and said at least one slice level holding circuit ~~causes~~ cause said at least one slice level to be held at said at least one substantially constant value for at least one prescribed time.

2. (Previously presented) The receiving apparatus according to claim 1, wherein said at least one variable gain amplifier serves as at least one bandpass filter.

3. (Currently amended) The receiving apparatus according to claim 1, wherein said at least one comparing circuit serves ~~as at least one gain switching detection circuit~~ to detect switching of said at least one gain.

4. (Previously presented) The receiving apparatus according to claim 1, wherein said at

least one time counted by said at least one counter circuit is variable.

5. (Previously presented) The receiving apparatus according to claim 1, wherein said at least one binarizing circuit comprises:

at least one minimum value detection circuit and at least one maximum value detection circuit accepting input of at least one demodulated signal from said at least one demodulator by way of at least one demodulated signal holding circuit and respectively detecting at least one minimum value and at least one maximum value of said at least one demodulated signal input thereto;

at least one adding circuit adding said at least one minimum value and said at least one maximum value;

at least one amplifier substantially halving at least one output of said at least one adding circuit; and

at least one comparing circuit carrying out binarization by comparing at least one magnitude of at least one output from said at least one amplifier and at least one magnitude of said at least one demodulated signal from said at least one demodulator;

said at least one demodulated signal holding circuit functioning as said at least one slice level holding circuit.

6. (Previously presented) The receiving apparatus according to claim 1, wherein said at least one binarizing circuit comprises:

at least one offset canceler circuit outputting, when at least one signal input thereto is less than at least one lower cutoff value, said at least one signal corresponding to at least one amount by which said at least one signal input thereto is less than said at least one lower cutoff value, and outputting, when said at least one signal input thereto is greater than said at least one upper cutoff value, said at least one signal corresponding to said at least one amount by which said at least one of the signal input thereto is greater than said at least one upper cutoff value;

at least one integrating circuits integrating said at least one output therefrom;

at least one offset canceler output holding circuit provided between said at least one

offset canceler circuit and said at least one integrating circuit;

at least one adding circuit adding and feeding back at least one output from said at least one integrating circuit to at least one input signal; and

at least one sign determining circuit using the sign of at least one signal output from said at least one adding circuit to carry out binarization;

said at least one offset canceler output holding circuit functioning as said at least one slice level holding circuit.

7. (Previously presented) The receiving apparatus according to claim 1, wherein said at least one binarizing circuit or circuits comprises:

at least one offset canceler circuit outputting, when at least one signal input thereto is less than at least one lower cutoff value, said at least one signal corresponding to at least one amount by which said at least one signal input thereto is less than said at least one lower cutoff value, or outputting, when said at least one signal input thereto is greater than said at least one upper cutoff value, said at least one signal corresponding to said at least one amount by which said at least one signal input thereto is greater than said at least one upper cutoff value;

at least one integrating circuit integrating said at least one output therefrom;

at least one offset canceler output holding circuit provided between said at least one offset canceler circuit and said at least one integrating circuit;

at least one adding circuit adding and feeding back at least one output from said at least one integrating circuit to at least one input signal; and

at least one sign determining circuit using the sign of at least one signal output from said at least one adding circuit to carry out binarization;

said at least one offset canceler output holding circuit functioning as said at least one slice level holding circuit.

8. (New) A receiving apparatus comprising:

a variable gain amplifier;

a level detection circuit for detecting an output of the variable gain amplifier;

a comparing circuit for comparing a reference level to said output from said level detection circuit and outputting a gain setting signal comprising a positive gain setting signal or a negative gain setting signal;

a demodulator;

a binarizing circuit;

a slice level holding circuit holding a slice level employed by said binarizing circuit at a substantially constant value; and

a counter circuit receiving a first input when said comparing circuit outputs the positive gain setting signal and a second input when said comparing circuit outputs the negative gain setting signal, the counter circuit being operatively connected to said slice level holding circuit;

said counter circuit causing said slice level holding circuit to hold the slice level at the substantially constant value for a given time when said first input changes to said second input or when said second input changes to said first input.

9. (New) The receiving apparatus according to claim 8, wherein said binarizing circuit comprises:

a minimum value detection circuit and a maximum value detection circuit accepting input of a demodulated signal from said demodulator by way of said slice level holding circuit and respectively detecting at least one minimum value and at least one maximum value of said at least one demodulated signal input thereto;

an adding circuit adding said minimum value and said maximum value;

an amplifier substantially halving an output of said adding circuit; and

a comparing circuit carrying out binarization by comparing a magnitude of an output from said amplifier and a magnitude of said demodulated signal from said demodulator.

10. (New) The receiving apparatus according to claim 8, wherein said binarizing circuit comprises:

an offset canceler circuit outputting, when an input signal input thereto is less than a lower cutoff value, an output signal corresponding to an amount by which said input signal is

less than said lower cutoff value, and outputting, when said input signal is greater than an upper cutoff value, an output signal corresponding to an amount by which said input signal is greater than said upper cutoff value;

an integrating circuit integrating said output signal;

an adding circuit adding and feeding back an output from said integrating circuit to said input signal; and

a sign determining circuit using the sign of a signal output from said adding circuit to carry out binarization;

wherein said slice level holding circuit is provided between said offset canceler circuit and said integrating circuit.

11. (New) A receiving apparatus comprising:

a variable gain amplifier;

a level detection circuit for detecting an output of the variable gain amplifier;

a comparing circuit for comparing a reference level to said output from said level detection circuit and outputting a gain setting signal comprising a positive gain setting signal or a negative gain setting signal;

a demodulator;

a binarizing circuit;

means for holding a slice level employed by said binarizing circuit at a substantially constant value; and

a counter circuit receiving a first input when said comparing circuit outputs the positive gain setting signal and a second input when said comparing circuit outputs the negative gain setting signal, the counter circuit being operatively connected to said means for holding a slice level employed by said binarizing circuit at a substantially constant value;

said counter circuit causing said means for holding a slice level employed by said binarizing circuit at a substantially constant value to hold the slice level at the substantially constant value for a given time when said first input changes to said second input or when said second input changes to said first input.

12. (New) The receiving apparatus according to claim 11, wherein said binarizing circuit comprises:

a minimum value detection circuit and a maximum value detection circuit accepting input of a demodulated signal from said demodulator by way of said means for holding a slice level employed by said binarizing circuit at a substantially constant value and respectively detecting at least one minimum value and at least one maximum value of said at least one demodulated signal input thereto;

an adding circuit adding said minimum value and said maximum value;

an amplifier substantially halving an output of said adding circuit; and

a comparing circuit carrying out binarization by comparing a magnitude of an output from said amplifier and a magnitude of said demodulated signal from said demodulator.

13. (New) The receiving apparatus according to claim 11, wherein said binarizing circuit comprises:

an offset canceler circuit outputting, when an input signal input thereto is less than a lower cutoff value, an output signal corresponding to an amount by which said input signal is less than said lower cutoff value, and outputting, when said input signal is greater than an upper cutoff value, an output signal corresponding to an amount by which said input signal is greater than said upper cutoff value;

an integrating circuit integrating said output signal;

an adding circuit adding and feeding back an output from said integrating circuit to said input signal; and

a sign determining circuit using the sign of a signal output from said adding circuit to carry out binarization;

wherein said means for holding a slice level employed by said binarizing circuit at a substantially constant value being provided between said offset canceler circuit and said integrating circuit.